

capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

- B1 word*
A3 word
- b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure;
 - c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;
 - d) forming a mask pattern over said cell node;
 - e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node;
 - f) removing the mask pattern;
 - g) forming a dielectric layer over said substrate; and
 - h) forming a bitline contact to said second bitline region.

8. (AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of :

- sub B2*
A4
- a) forming a dielectric layer on a substrate;
forming a conductive layer on said dielectric layer;
patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;
 - (1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

- A4
lined*
- C3
lined*
- (2) said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between $1E17$ and $1E18$ atoms/cc;
- b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region and said first bit line region do not intersect;
- (1) said first bit line region and said cell node region have a p-type doping and have an impurity concentration between $1E18$ and $1E19$ atoms/cc,
- c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;
- d) forming a mask pattern over said cell node;
- e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node; said second bitline region has a concentration between $1E20$ and $1E21$ atom/cc;
- f) removing the mask pattern;
- g) forming a dielectric layer over said substrate; and
- h) forming a bitline contact to said second bitline region.

Please cancel claims 9 to 14

Please add new claims as shown below:

- A5*
15. A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:

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- a) forming a dielectric layer on a substrate;
 - b) forming a conductive layer on said dielectric layer;
 - c) patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;
 - d) forming a word line structure and a capacitor plate structure on a substrate;
 - (1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;
 - e) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region;
 - f) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;
 - g) forming a mask pattern over said cell node;
 - h) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node;
 - i) removing the mask pattern;
 - j) forming a dielectric layer over said substrate; and
 - k) forming a bitline contact to said second bitline region.